

THE UNITED STATES PATENT AND TRADEMARK OFFICE

FS BED HS-02

n re Application of:

Rogers et al.

Examiner: Rose, Kiesha L.

Serial No.: 09/825,027 //) Art

Art Unit: 2822

Filed:

04/02/01

For: CLOCKED BASED METHOD AND DEVICES FOR MEASURING VOLTAGE-VARIABLE CAPACITANCES AND OTHER NON-CHIP PARAMETERS

Assistant Commissioner of Patents and Trademarks Washington, D.C. 20231

Dear Sir:

RESPONSE TO RESTRICTION REQUIREMENT

In the Office Action mailed May 6, 2002, the Examiner has stated that the present Application contains two distinct inventions related as a process of making and a product made. As such, the Examiner has required Applicants to elect a single invention for prosecution on the merits. Specifically, the Examiner has required Applicants to elect between a first invention, Group I, recited in Claims 1-29 and 73-108, drawn to a semiconductor device, classified in class 257, subclass 324; and a second invention, Group II, recited in Claims 30-72, drawn to a method of making a semiconductor device, classified in class 438, subclass 1+.

AMD-E1019

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ELECTION WITHOUT TRAVERSE BETWEEN GROUP I AND GROUP II

Applicants elect without traverse Group I, recited in Claims 1-29 and 73-108, drawn to a semiconductor device, classified in class 257, subclass 324, classified in class 257, subclass 324.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Date: 6/5/02

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